M64100TFP

ON-VEHICLE LAN CONTROLLER

DESCRIPTION

The M64100TFP is an on-vehicle LAN controller, which supports the CSMA/CD-based competitive bus control mode.

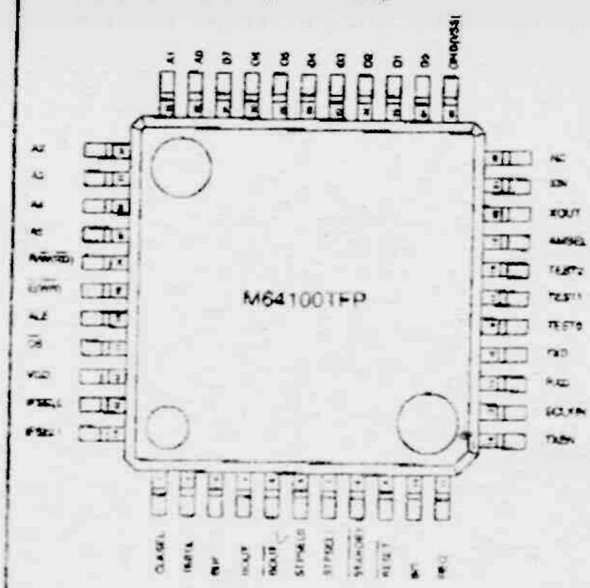
This LAN controller is provided with a one-frame transmitter buffer and receiver buffers. These buffers are independent. The LAN controller only receives message frames directed to the current node, reducing the burden loaded on the control microcomputer and carrying out high-speed transmission control.

The protocol control and frame format of the M64100TFP comply with SAE-J1850.

FEATURES

- Protocol control compliant with SAE-J1850
- Collision detection and priority control by CSMA/CD
- The address filter function makes it possible to receive only message frames containing the address of the current node.
- Three transfer rates are supported (20.8 kbps/41.6 kbps/125 kbps). (Settings are made by an external oscillator and the frequency division-ratio setting pin.)
- Uses the PWM mode for coding and decoding of signals sent to and from transmission line
- Built-in 8-bit CRC coder and decoder for error detection
- Built-in 1-frame transmitter buffer and receiver buffers for 2 frames
- Supports the 1-byte response (IFR) mode (automatic IFR transmit-receive function built in)
- A reception address, as well as a physical address, can be set as destination address
- Supports analyzer reception
- Status register facilitates the microcomputer to detect every transmission condition
- The frame format complies with the 3-byte header, 1-receiver node and 1-byte response mode of SAE-J1850. Frame length is variable up to 12 bytes (including a response byte).
- Various kinds of microcomputer interfaces built in
  - Clock-sync serial interface (LSB first 8 bits data)
  - UART interface
    (LSB first, 1 start bit + 8 bits data + (1 parity bit) + 1 stop bit)
    Choice of with or without parity bit
    Automatic conversion: LSB first format to MSB first format when sending to BUS line; when receiving from BUS line, from MSB first format to LSB first format
  - Parallel interfaces (2 kinds)
- Built-in error detection functions for various kinds of transmission errors
  - Transmission errors
    SOF error, echo back error, IFR bit error, no IFR error, IFR disparity error, improper IFR length error
  - Reception errors
    Double address definition error, CRC error, improper message length error, bit error, byte error
- Standby mode supported
  - Standby mode enterable set by control microcomputer (power dissipation at standby mode ISTBY ≤ 150 µA)

PIN CONFIGURATION (TOP VIEW)



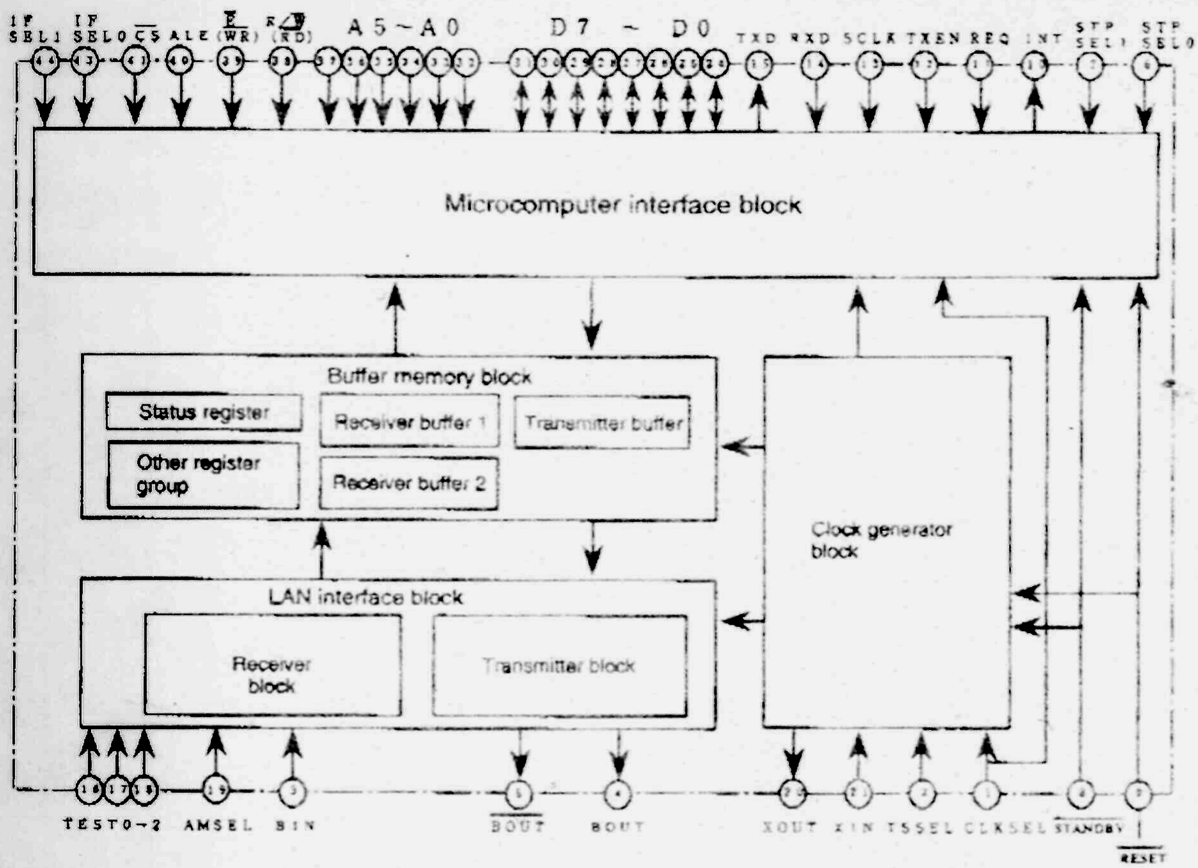
Outline: 44P6N-A

- When the BIN pin input waveform is found to make a rise in the standby mode, this controller commands control microcomputer to cancel the mode (wakeup time ≤ 11ms)

APPLICATION

On-vehicle LAN

BLOCK DIAGRAM of M64100TFP



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DESCRIPTION OF PIN

<table>
<tr><th>Pin No.</th><th>Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>①</td><td>CLKSEL</td><td>Input</td><td>Input pin for system clock selection
<table><tr><td>L</td><td>For 6 MHz clock input frequency</td></tr><tr><td>H</td><td>For 2 MHz clock input frequency</td></tr></table></td></tr>
<tr><td>②</td><td>TSSEL</td><td>Input</td><td>Input pin for transfer rate setting for exchange with BUS line
<table><tr><th>Clock input</th><th>TSSEL</th><th>Transfer rate</th></tr>
<tr><td rowspan="2">6MHz
(CLKSEL = L)</td><td>L</td><td>125Kbps</td></tr>
<tr><td>H</td><td>41.6Kbps</td></tr>
<tr><td rowspan="2">2MHz
(CLKSEL = H)</td><td>L</td><td>41.6Kbps</td></tr>
<tr><td>H</td><td>20.8Kbps</td></tr></table></td></tr>
<tr><td>③</td><td>BIN</td><td>Input</td><td>Input pin for signals received from BUS line</td></tr>
<tr><td>④</td><td>BOUT</td><td>Output</td><td>Positive logic signal output pin for transfer to BUS line (message frame for transmission)</td></tr>
<tr><td>⑤</td><td>$\overline{\text{BOUT}}$</td><td>Output</td><td>Negative logic signal output pin for transfer to BUS line (message frame for transmission)</td></tr>
<tr><td>⑥

⑦</td><td>STPSEL0

STPSEL1</td><td>Input

Input</td><td>Parity check setting pins effective when using UART interface for the interface with control microcomputer
<table><tr><th>STPSEL0</th><th>STPSEL1</th><th>Function</th></tr>
<tr><td>L</td><td>L</td><td>Odd parity</td></tr>
<tr><td>H</td><td>L</td><td>Even parity</td></tr>
<tr><td>—</td><td>H</td><td>No parity</td></tr></table></td></tr>
<tr><td>⑧</td><td>$\overline{\text{STANDBY}}$</td><td>Input</td><td>Standby mode setting pin used by control microcomputer
L: standby mode/H: operating mode</td></tr>
<tr><td>⑨</td><td>$\overline{\text{RESET}}$</td><td>Input</td><td>Reset input pin used by control microcomputer
L: reset mode/H: operating mode</td></tr>
<tr><td>⑩</td><td>INT</td><td>Output</td><td>Output pin for handshake with control microcomputer
See "Communications with the Control Microcomputer" on and after page 17 for details.</td></tr>
<tr><td>⑪</td><td>REQ</td><td>Input</td><td>Input pin for handshake with control microcomputer
See "Communications with the Control Microcomputer" on and after page 17 for details.</td></tr>
<tr><td>⑫</td><td>TXEN</td><td>Input</td><td>Input pin for control of serial interface
When using a serial interface, fix this pin to "H."</td></tr>
<tr><td>⑬</td><td>SCLKIN</td><td>Input</td><td>Clock input signal for the use of the clock sync serial interface</td></tr>
<tr><td>⑭</td><td>RXD</td><td>Input</td><td>Functions as serial data input pin when using a serial interface (LSB first).</td></tr>
<tr><td>⑮</td><td>TXD</td><td>Output</td><td>Functions as serial data output pin when using a serial interface (LSB first).</td></tr>
<tr><td>⑯
⑰
⑱</td><td>TEST0
TEST1
TEST2</td><td>Input</td><td>Test input pins.
Usually, fix pins 16, 17, and 18 to "L."</td></tr>
<tr><td>⑲</td><td>AMSEL</td><td>Input</td><td><table><tr><td>L</td><td>Normal transmission</td></tr><tr><td>H</td><td>Receives all message frames on BUS line</td></tr></table></td></tr>
<tr><td>⑳</td><td>XOUT</td><td>Output</td><td>Oscillator output pin</td></tr>
<tr><td>㉑</td><td>XIN</td><td>Input</td><td>Oscillator input pin</td></tr>
</table>

DESCRIPTION OF PIN (Continued)

<table>
<tr><th>Pin No.</th><th>Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>22</td><td>NC</td><td>—</td><td>Connected to GND in normal use.</td></tr>
<tr><td>23</td><td>GND</td><td>Input</td><td>Grounding pin</td></tr>
<tr><td>24
25
26
27
28
29
30
31</td><td>D0
D1
D2
D3
D4
D5
D6
D7</td><td>Input/
Output</td><td>Function as data bus I/O pins when using a parallel interface</td></tr>
<tr><td>32
33
34
35
36
37</td><td>A0
A1
A2
A3
A4
A5</td><td>Input</td><td>Function as address bus input pins when using a parallel interface</td></tr>
<tr><td>38
39</td><td>$R/\overline{W}$ ($\overline{RD}$)
$\overline{E}$ ($\overline{WR}$)</td><td>Input
Input</td><td><table>
<tr><th>IFSEL0</th><th>IFSEL1</th><th>Interface type</th><th>Pin 38</th><th>Pin 39</th></tr>
<tr><td>L</td><td>H</td><td>Parallel interface 1</td><td>$R/\overline{W}$ mode</td><td>$\overline{E}$ mode</td></tr>
<tr><td>H</td><td>H</td><td>Parallel interface 2</td><td>$\overline{RD}$ mode</td><td>$\overline{WR}$ mode</td></tr>
</table></td></tr>
<tr><td>40</td><td>ALE</td><td>Input</td><td>Address latch signal for parallel interface (address latch at falling edge)</td></tr>
<tr><td>41</td><td>$\overline{CS}$</td><td>Input</td><td>Device selector pin
L: select H: unselect</td></tr>
<tr><td>42</td><td>VDD</td><td>Input</td><td>Power supply input pin</td></tr>
<tr><td>43
44</td><td>IFSEL0
IFSEL1</td><td>Input
Input</td><td>Interface setting pins for interfacing with control microcomputer<table>
<tr><th>IFSEL0</th><th>IFSEL1</th><th>Interface type</th></tr>
<tr><td>L</td><td>L</td><td>Clock sync serial interface</td></tr>
<tr><td>H</td><td>L</td><td>UART interface</td></tr>
<tr><td>L</td><td>H</td><td>Parallel interface 1</td></tr>
<tr><td>H</td><td>H</td><td>Parallel interface 2</td></tr>
</table>Parallel interface 1 = A/D bus multiplex type
Parallel interface 2 = A/D bus separation type</td></tr>
</table>

COMMUNICATION FUNCTIONS

DESCRIPTION OF COMMUNICATION FUNCTIONS

The LAN controller, temporarily storing data sent from the control microcomputer, forms a message frame and also monitors the status of the BUS line. When the LAN controller finds the BUS line in transmittable condition, it sends the message frame to the BUS line.

When the LAN controller detects a message frame directed to the current node, it receives the message frame and checks to see if there is a reception error occurring. Next, storing the message frame in the receiver buffer as received data, the LAN controller transfers the data to the control microcomputer.

(The section "Communication with the Control Microcomputer" on and after page 17 deals with data transfer between the control microcomputer and the LAN controller.)

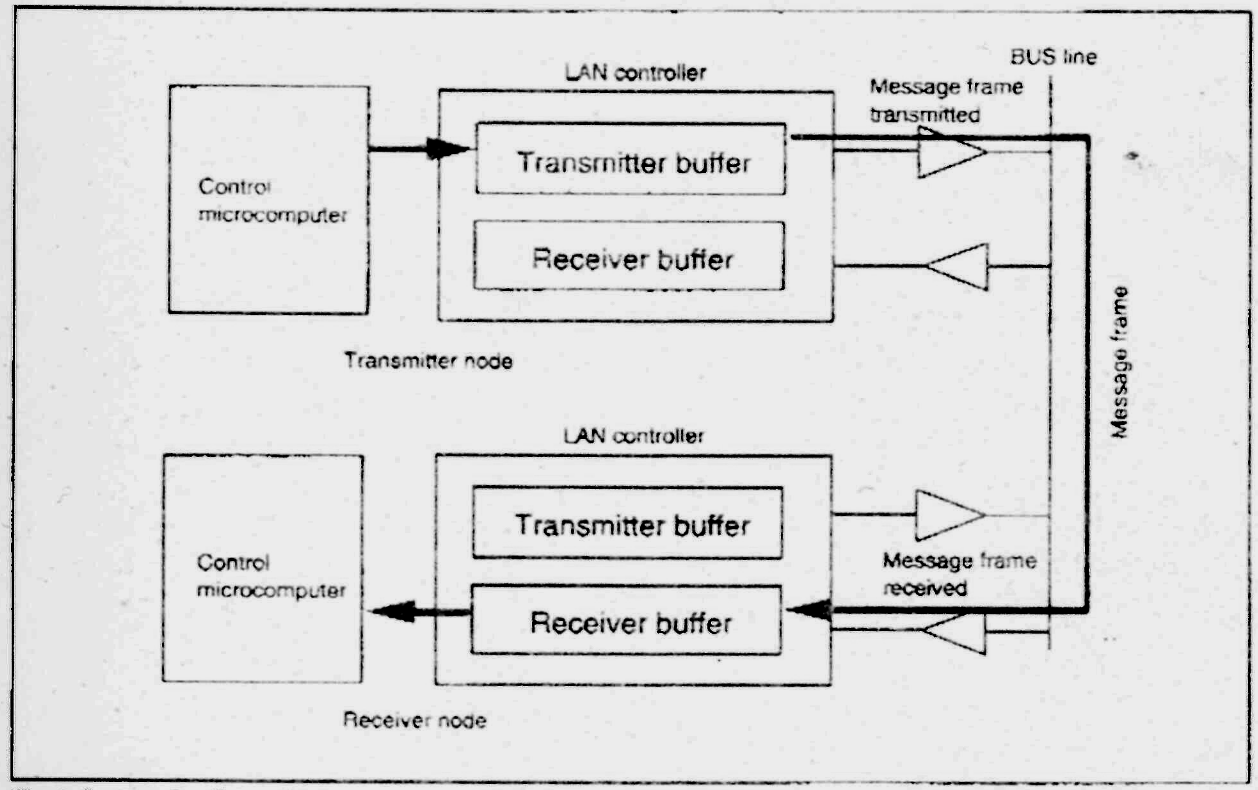
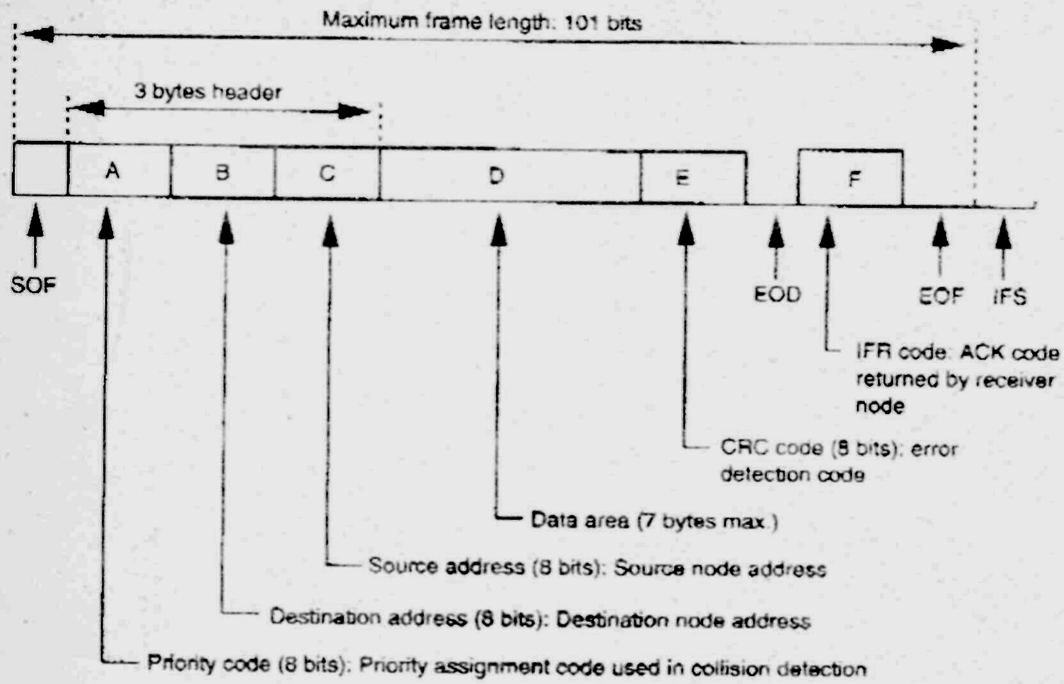


Fig. 1 System Configuration

COMMUNICATION FORMAT
FRAME FORMAT

The frame format this LAN controller handles complies with the 1-receiver node and 1-byte response (IFR) type of SAE-J1850. The basic frame format is illustrated in Fig. 2.



- Data area D is variable in length from 1 to 7 bytes.
- CRC code E is added to the last segment of the data contained in the data area when the LAN controller has carried out 8-bit CRC operation for A, B, C, and D.

Note SOF: Start Of Frame
EOD: End Of Data
EOF: End Of Frame
IFS: Inter Frame Separation

Fig. 2 Frame Format

BIT FORMAT

The LAN controller supports the PWM bit format of SAE-J1850. Fig. 3 shows each kind of bit and symbols.

The data bit format shown in (2) is used for segments A through F of the frame format specified in previous page. One bit consists of 3 time zones. Data "0" corresponds to 2 time zones of "H" level plus 1 time zone of "L" level. Data "1" corresponds to 1 time zone of "H" level and 2 time zones of "L" level. The structure of each symbol is as shown in Fig. 3.

The LAN controller takes the data stored in the transmitter buffer to form the frame format shown in Fig. 2, encodes the data into the bit format shown in Fig. 3, and transfers to the BUS line.

The LAN controller of a receiver node decodes message frames sent through BUS line. When the LAN controller identifies a certain message frame as one directed to the current node, it carries out reception process for the message frame.

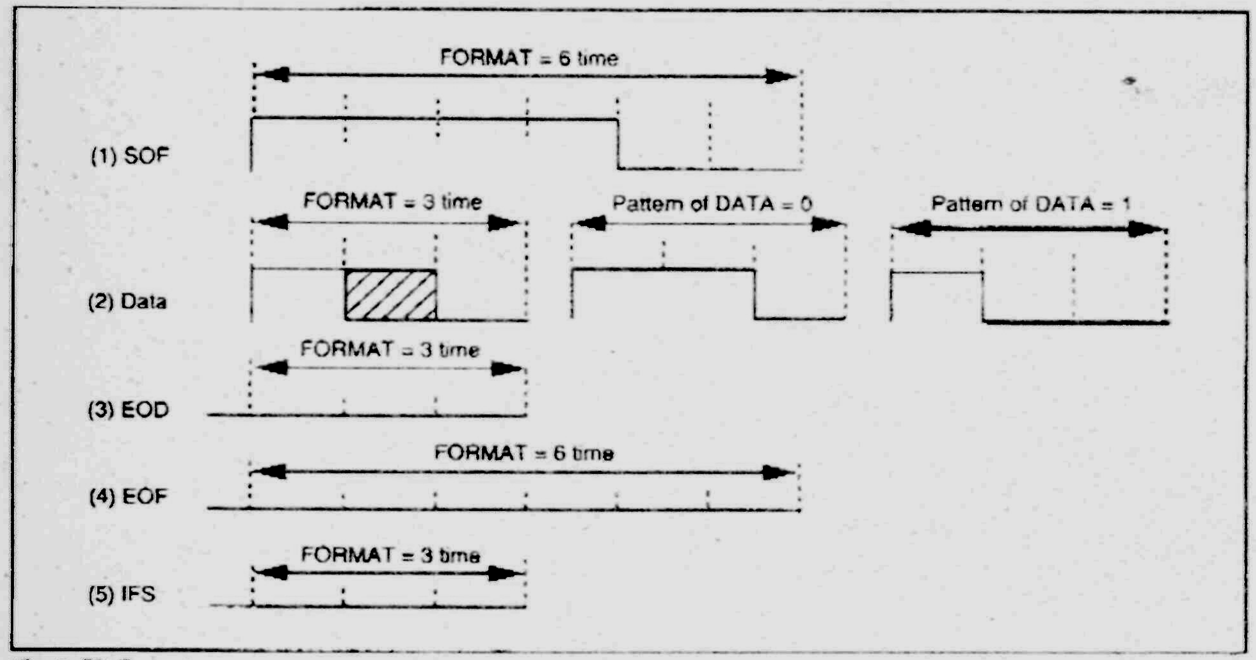


Fig. 3 Bit Format

TRANSFER RATE SETTING METHOD

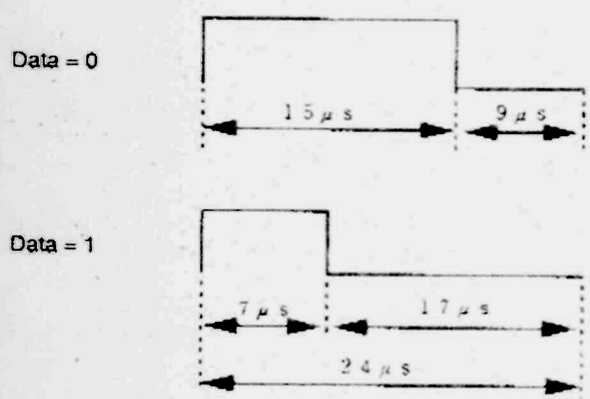
The LAN controller has a built-in oscillator circuit, which uses a 6MHz or 2MHz ceramic or quartz resonator. Transmission is carried out timed by 6MHz or 2MHz clock signals, which are generated by the oscillator.

For transfer rates, two kinds of settings are available for each clock mode, arranging the TSSEL and CLKSEL pins. Table 1 shows the available settings.

Table 1 Transfer Rate Setting Method

Clock mode	CLKSEL	TSSEL	Transfer rate	Clock input ratio
Clock frequency 6MHz	L	L	125kbps	1/48
		H	41.6kbps	1/144
Clock frequency 2MHz	H	L	41.6kbps	1/48
		H	20.8kbps	1/96

As shown above, the combination of the CLKSEL and TSSEL pins permits to select from two kinds of transfer rates with one type of clock input. If 41.6 kbps is selected, bit timing of transferred data will be as follows.



PRIORITY CONTROL FUNCTION (COLLISION DETECTION FUNCTION)

The LAN controller carries out priority control by collision detection. When sending a message frame, it compares the data sent from the current node with the data on the BUS line, detecting through the BIN pin. This mechanism is shown in Fig. 4.

When two or more nodes are to transmit data to the BUS line, the priority control function gives priority to one of them. This function checks the priority code. Only the node that is given priority can send a message frame to the BUS line. If each message frame sent from each of plural nodes has the same priority code, priority is given checking the second byte (destination address) and following information. The node that could not obtain priority due to priority control reattempts to send automatically. If a node fails in obtaining priority even after 3 times of attempts, it notices the control microcomputer a transmission error. Then, the control microcomputer ought to execute another transmission process (writing transmission data on the transmitter buffer). It is probable that even the new message frame results in a transmission error without gaining priority, so it is recommended to select a higher priority code for the message frame.

The chart shown in Fig. 5 illustrates the relationship between priority codes and priority.

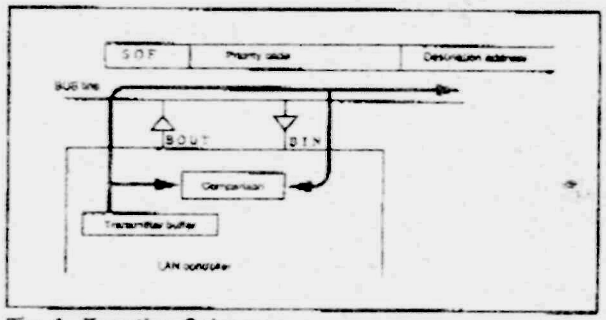


Fig. 4. Function Scheme

Priority code								Priority
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	High
0	0	0	0	0	0	0	1	↑
			⋮					
1	1	1	1	1	1	1	0	
1	1	1	1	1	1	1	1	Low

Fig. 5. Priority Code Chart

To explain the priority control, Fig. 6 is used.

In the figure, Nodes A and B are issuing a transfer request. If the priority codes of Nodes A and B are configured as A5 (H) and B5 (H), respectively, Node B detects that the data it is sending differs from the data on the BUS line at the 4th bit (collision detection). Then, Node B stops transmission. Node A is given priority and continues to send its message frame.

ADDRESS FILTERING 1

Address filtering is a function that the LAN controller checks message frames on the BUS line and screens for data frames addressed to the current node as message frames to be processed. This function eliminates the need for the control microcomputer to identify whether message frames on the BUS line are sent to the current node, so software tasks of the control microcomputer are reduced.

As shown in Fig. 7 illustrating the function, the LAN controller makes decision to receive a message frame when it compares the second byte (destination address) of the frame format with the preset physical address and finds them coinciding. The example shows that Node A sends Node B a message frame. The second byte of the message frame is set to "02 (H)." Node B, whose physical address is preset to "02 (H)," judges the frame to be directed to itself and begins reception process. Node C, whose physical address is preset to "03 (H)," makes judgement that the message frame is not addressed to its node and executes no process for reception. (For the physical address setting method, see "Communications with the Control Microcomputer," on and after page 17.)

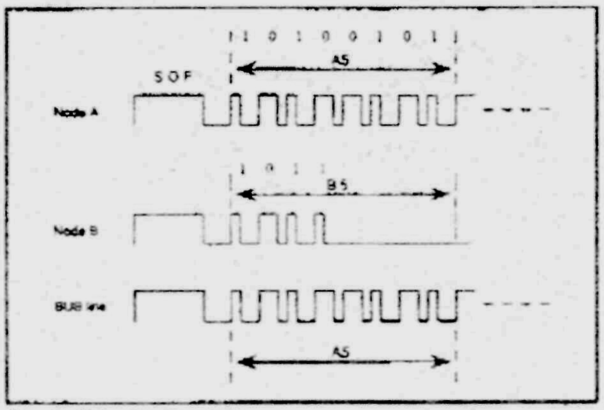


Fig. 6 Priority Control

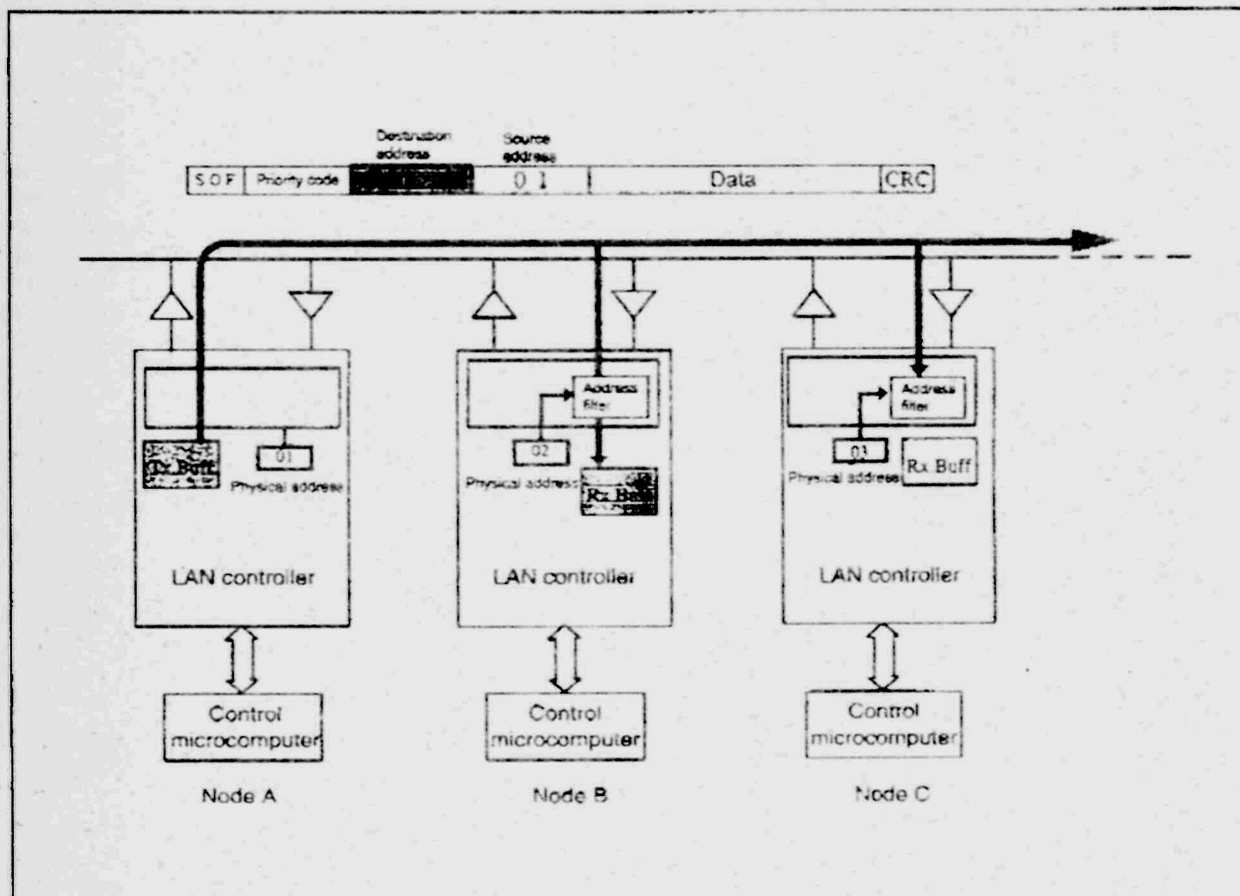


Fig. 7 Address Filtering

ADDRESS FILTERING 2

The M64100TFP permits another address setting (called reception address) in addition to physical address, to check whether to receive message frames on the LAN transmission line.

The LAN controller performs reception process if its reception address coincide with the second byte (destination address) of a message frame on the BUS line. If no reception error listed in the section "Reception Error Register 32 (H)" on page 16 is detected in the received frame, the LAN controller returns an IFR. The information written in the IFR at that time is the data written in the physical address. The details of IFR will be explained in the section "IFR (Response) Automatic Return Function" on page 10.

In a case that two or more nodes have the same reception address set, they at once perform reception process with a single message frame. It is then probable that the plural nodes that received the message frame and detected no reception errors listed in the section "Reception Error Register 32 (H)" on page 16 will return IFR. As the LAN controller performs priority control by collision detection also for the returning IFR segment, the node that has selected a smaller value for its physical address will successfully return the IFR to the source transmitter node. If a node detects collision and stops returning IFR, however, proper reception process is performed.

As a node that transmits a message frame directing to a reception address will detect the disagreeing IFR error (included in the transmission errors listed in the section "Transmission Error Register 31 (H)" on page 15), the control microcomputer can judge it a pseudo error.

If a node writes the same information as its own reception address into the second byte (destination address) of the transmitter buffer and transmits the message frame, the LAN controller performs transmission and reception process at once with the same message frame. In such a case the LAN controller, while performing reception process, detects the double address definition error included in the reception errors listed in the section "Reception Error Register 32 (H)" on page 16. After that, it proceeds to the reception error process.

(For the reception address setting method, see "Register Configuration," page 12.)

IFR (RESPONSE) AUTOMATIC RETURN FUNCTION

As explained in sections "Address Filtering 1" on page 9 and "Address Filtering 2" on page 10, the LAN controller, with the address filtering function, detects message frames directed to the current node and proceeds to reception process. If no reception error is detected with the received message frame, the LAN controller stores the received data in the receiver buffer and at the same time sends back an IFR as ACK to the transmitter node to notify proper reception. This IFR code is the physical address preset to the receiver node. If a reception error is detected in the received frame, the LAN controller sends back no IFR. The transmitter node will recognize that the transmission was not properly executed as no IFR returns.

Fig. 8 shows that the frame on the BUS line is a message frame consisting of a frame transmitted from Node A plus the IFR of receiver Node B.

OVERRUN PROCESSING FUNCTION

The LAN controller has receiver buffers for 2 frames. Overrun occurs when a frame is sent to a node before the

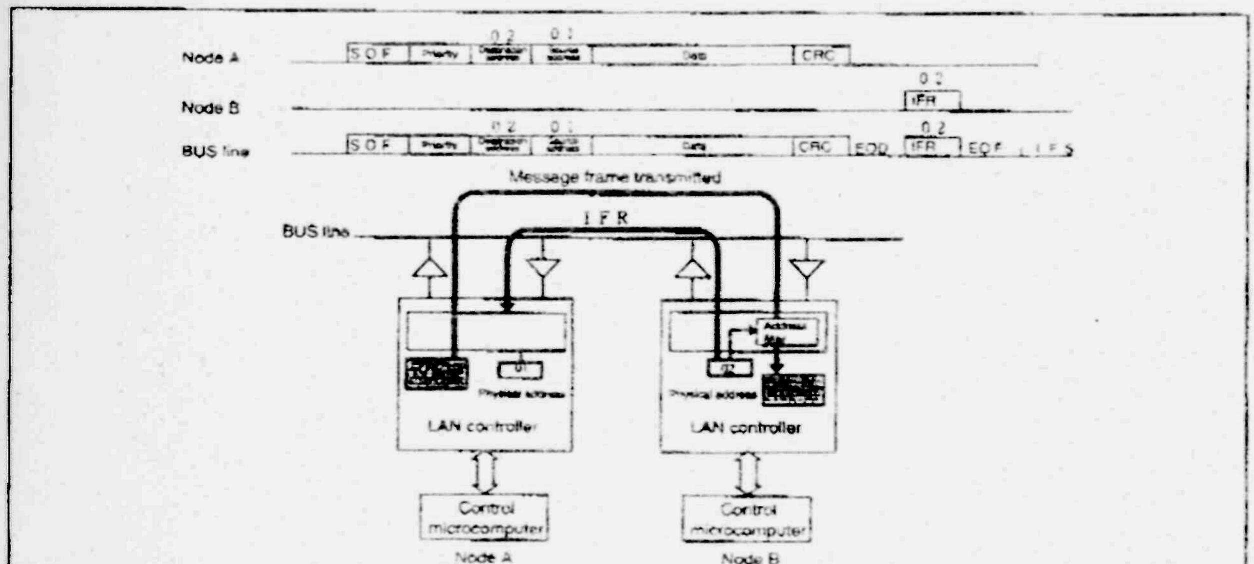


Fig. 8 RSP Return Function

OVERRUN PROCESSING FUNCTION

The LAN controller has receiver buffers for 2 frames. Overrun occurs when a frame is sent to a node before the control microcomputer reads out the received frames already stored in the buffers of 2 frames. In that case no buffer is available for storing the data contained in the received frames. The LAN controller, however, stores as overrun source address the third byte contained in the message frame, that is, the source address (the physical address of the node that sent the frame). The control microcomputer recognizes the occurrence of the overrun from the status data as well as which node has sent the message. For how to read the overrun source address, see "Communications with the Control Microcomputer" on and after page 17.

ANALYZER FUNCTION

Setting the AMSEL pin (pin 19) to "H" disables the address filtering function, then the LAN controller performs reception process for all frames on the BUS line. When the LAN controller is in this mode it returns no IFR so it does not obstruct communications between other nodes.

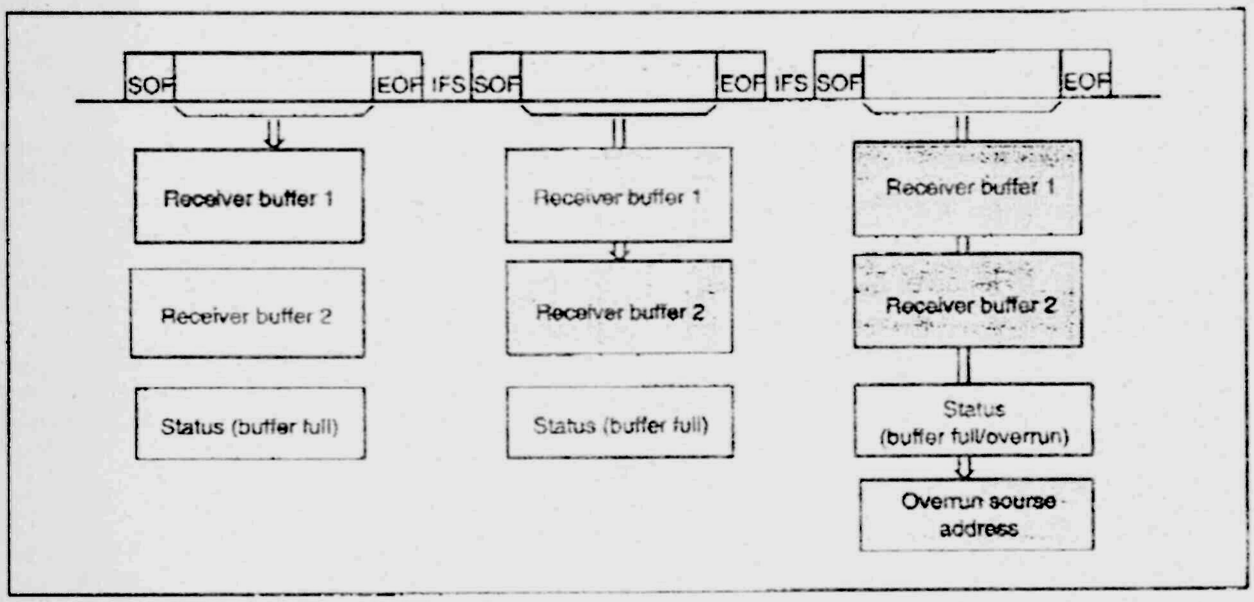


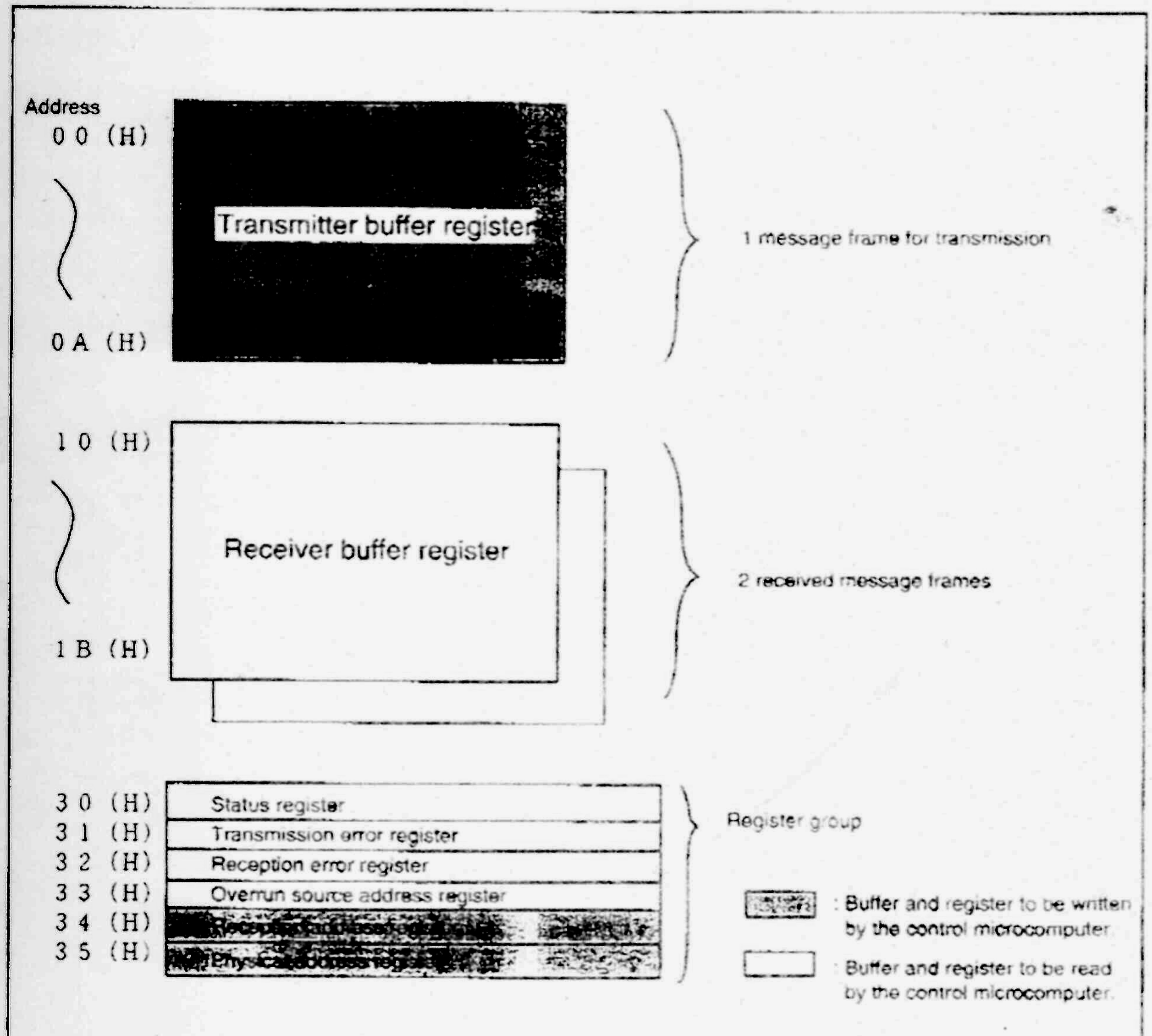
Fig. 9 Overrun Processing

REGISTER CONFIGURATION

GENERAL CONFIGURATION OF BUFFER REGISTERS

This section deals with each register and buffer memory in the LAN controller. Fig. 10 shows a general form of the registers and buffer memory.

In Fig. 10, the LAN controller comprises a transmitter buffer register for one frame and receiver buffer registers for two frames. It also includes 6 more registers. Each buffer register and other registers will be explained in the section "Transmission Buffer Register" on and after page 13.



Note: In the following descriptions, (H) denotes expression in hexadecimal, while (B) denotes the binary system.

An example of expression in the binary system is XXXXXXXX (MSB … LSB) (X stands for 0 and 1.)

Fig. 10

TRANSMITTER BUFFER REGISTER

The LAN controller forms a message frame for transmission from the data written in the transmitter buffer register, and sends the message frame to the BUS line. Fig. 11 illustrates the relationship between the configuration of the transmitter buffer register and message frame for transmission.

It is necessary to write the number of bytes from the priority code to data n as the transmission frame length. The LAN controller carries out CRC operation for the data from the priority code through data n and adds the result as an 8-bit CRC code after data n in the message frame for transmission.

If a parallel interface is used, it is necessary to designate address to write data. When using a serial interface, no consideration is required for address to write data. For details, see "Communication with the Control Microcomputer," pages 25 and 47, which deals with how to write transmission data.

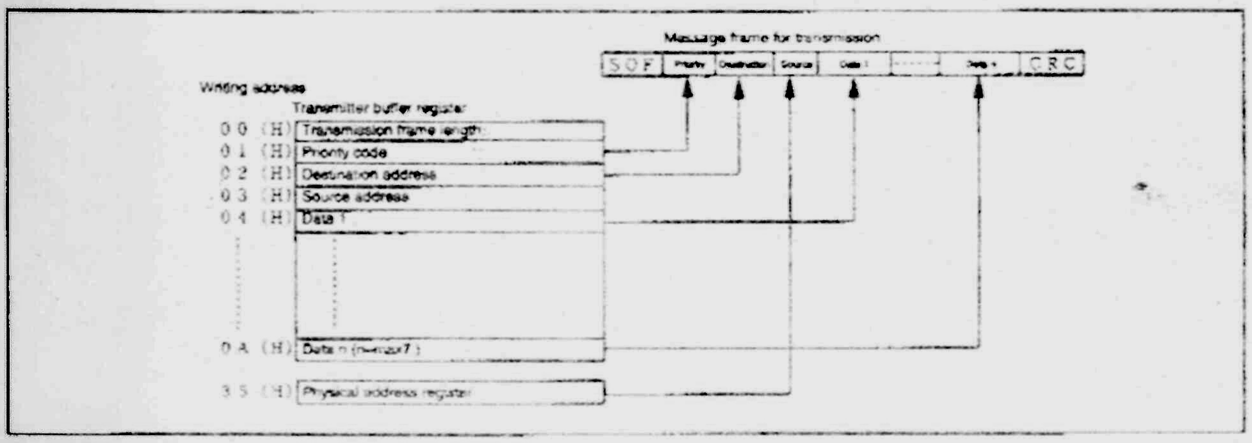


Fig. 11 Transmitter Buffer Register

RECEIVER BUFFER REGISTER

If the second byte (destination address) of a message frame on the BUS line coincides with the physical address of the current node, the LAN controller handles the message frame as a frame to be received and stores the data contained in that frame in the receiver buffer.

The LAN controller has receiver buffer registers for 2 frames. The control microcomputer need not recognize in which register data is stored.

The LAN controller counts the number of bytes from the priority code through the CRC byte and writes to address 10 (H) of the receiver buffer.

The CRC byte is stored next to the address of data n. When n = 2, for example, the CRC byte is stored to address 16 (H).

After carrying out reception properly (reception with no reception error, which will be explained later), the LAN controller automatically sends back the information stored in the physical address register as IFR. For details of how to read out received data, see "Communication with the Control Microcomputer," pages 27 and 48.

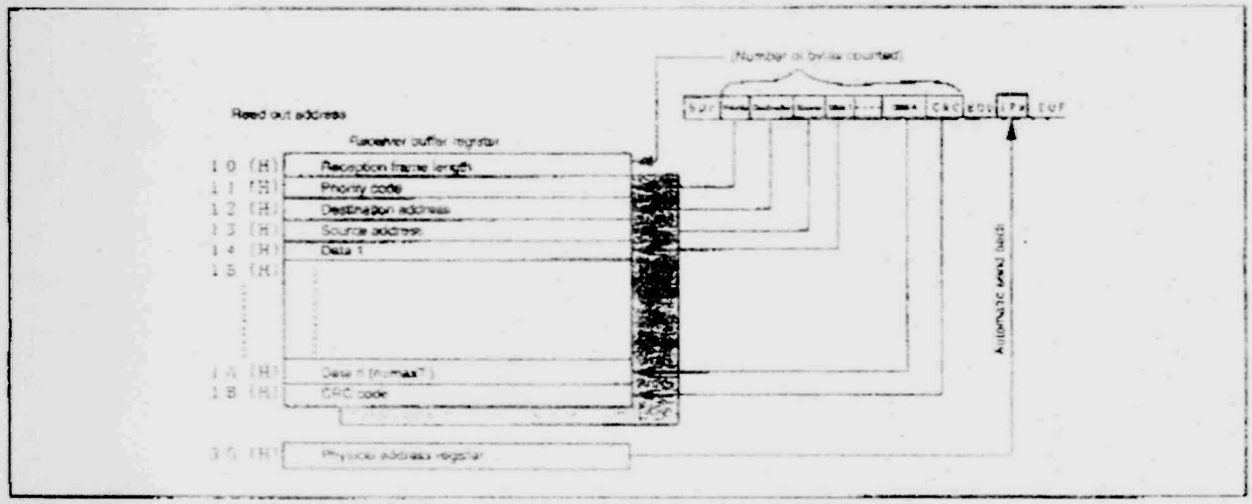
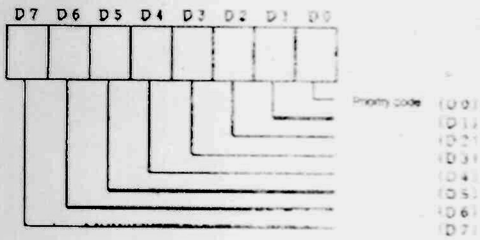


Fig. 12 Receiver Buffer Register

EACH REGISTER IN TRANSMITTER AND RECEIVER BUFFERS

Priority Codes

Priority code in the transmitter register: 01 (H)
Priority code in the receiver register: 11 (H)



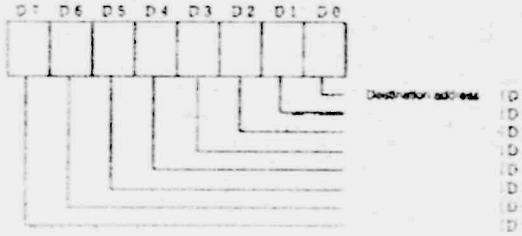
Priority code								Priority
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	High
0	0	0	0	0	0	0	1	
0	0	0	0	0	0	1	0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
1	1	1	1	1	1	1	0	
1	1	1	1	1	1	1	1	Low

All information in the priority code area is checked for collision detection when sending data. If the priority codes checked are the same, following data bytes, that is, the destination address and other bytes, are checked for collision detection. If a collision occurs on the BUS line and the transmission fails, the LAN controller automatically retries transmission after the data frame given priority is completely transmitted. If a node fails in transmitting a message frame three times successively, the LAN controller notifies the control microcomputer of a echo-back error.

DESTINATION ADDRESS

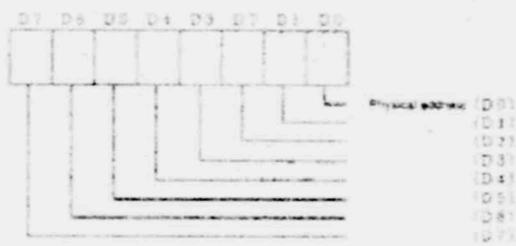
(1) Destination Address in the Transmitter Buffer Register: 02 (H)
When sending a message frame through the BUS line, the address (the content of the physical address register or the reception address register) of the destination node to which it is desired to send, is written in the transmitter buffer register.

(2) Destination Address in the Receiver Buffer Register: 12 (H)
The LAN controller compares the data of the second byte (destination address) in a message frame on the BUS line with the data in the physical address register of the current node or with the data in the reception address register. If they coincide, the LAN controller performs reception process to handle the message frame as a frame to be received. In other words, the destination address data in the receiver buffer should coincide with the data in the physical address register or the reception address register of the current node.



Physical Address Register: 35 (H)

The data written in the physical address register is the source address of that node. When a message frame for transmission is formed, that data is copied to the third byte of the message frame. Comparing the data in the physical register and the second byte (destination address) of a message frame on the BUS line, the LAN controller makes decision as to whether that message frame is directed to the current node. If they are the same, the LAN controller handles it as a message frame to be received. To this end, the physical address should be written after the LAN controller is freed from resetting. The data in the physical address register is 00 (H) immediately after it is freed from resetting or standby mode. For how to write a physical address, see "Communication with the Control Microcomputer," page 24.



DATA 1-n REGISTER

04-0 (n + 3) (H) in transmitter buffer register
14-1 (n + 3) (H) in receiver buffer register
n is variable from 1 to 7
(n = number of data bytes)

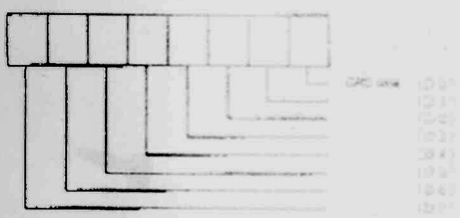
The data register has a variable-length format. It is capable of handling 1 to 7 bytes of data for transmission or reception.

CRC CODE: 1 (n + 4) (H)

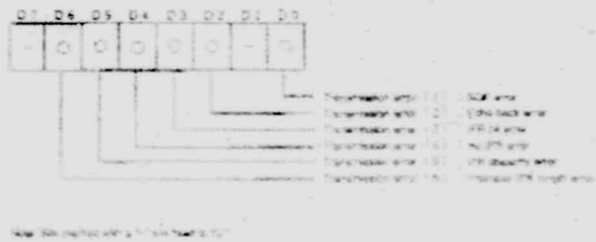
n = number of data bytes

The CRC code is stored to the address following the last data in the receiver buffer register. Prior to processing a received message frame, the LAN controller conducts the cyclic redundancy check (CRC) on the data, namely, from the priority code to the CRC code, to detect any error. (Since the CRC code, too, is stored in the receiver buffer register, it is possible for the control microcomputer to perform CRC error detection.)

In forming a message frame for transmission, on the other hand, the LAN controller carries out CRC calculation on data from priority code through data n, and the result is automatically sent as CRC code. The control microcomputer is free from CRC calculation for the data contained in a message frame for transmission.



TRANSMISSION ERROR REGISTER: 31 (H)



Transmission error: If a transmission error is detected when sending a message frame to the BUS line, the details of the error is stored in the transmission error register, address 31 (H) on the memory map.

Table 2 shows details of transmission errors.

Table 2 Details of Transmission Errors

Bit	Name	Condition	Reset condition
D0	SOF error	No SOF is detected in message frame for transmission.	After the control microcomputer reads out the transmission error register.
D2	Echo back error	This error is detected when a transmission message frame is rejected three times successively due to collision with other data and cannot be normally transmitted by the automatic retrial function (after automatic reattempts).	Same as above *
D3	IFR bit error	Detection in returned IFR of a waveform not included in the bit format.	Same as above
D4	NO IFR error	No IFR is returned.	Same as above
D5	IFR disparity error	The returned IFR does not coincide with the second byte (destination) of the transmitted message frame.	Same as above
D6	Improper IFR length error	The returned IFR does not consist of 8 bits.	Same as above

* D1 and D7 are fixed to "L."